UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER OF PATENTS AND TRADEMARKS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/653,541	08/31/2000	Mark Tuttle	M4065.0363/P363	4204

24998 7590 05/09/2003

DICKSTEIN SHAPIRO MORIN & OSHINSKY LLP
2101 L STREET NW
WASHINGTON, DC 20037-1526

EXAMINER	
HO, TU TU V	

ART UNIT	PAPER NUMBER
2818	

DATE MAILED: 05/09/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)
	09/653,541	TUTTLE, MARK
	Examiner	Art Unit
	Tu-Tu Ho	2818

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *21 March 2003* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-8,11,13-31,64-76 and 79-86* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-8,11,13-31,64-76 and 79-86* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *21 March 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) *18* .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after allowance or after an Office action under *Ex Parte Quayle*, 25 USPQ 74, 453 O.G. 213 (Comm'r Pat. 1935). Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, prosecution in this application has been reopened pursuant to 37 CFR 1.114. Applicant's submission filed on 17 and 21 March 2003 has been entered.

Claim Rejections

Note that the figures and reference numbers referred to in this office action are used merely to indicate an example of a specific teaching and are not to be taken as limiting.

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless --

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

(e) the invention was described in
(1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or
(2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

The following is a quotation of 35 U.S.C. §103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1-8, 11, 13-31, 64-76, 83-86, and 79-82 are rejected under 35 U.S.C. 102(b) as anticipated by or, in the alternative, under 35 U.S.C. 103(a) as obvious over Bright et al. U.S. Patent 5,357,404 (patent '7404), using common knowledge in the art or in view of Nakagawa et al. U.S. Patent 4,801,489 (patent '489), Juskey et al. U.S. Patent 5,371,404 (patent '1404), Higgins, III U.S. Patent 5,639,989 (patent '989), Gore et al. U.S. Patent 6,105,226 (patent '226), or Tracy et al. U.S. Patent 5,902,690 (cited by Applicant, and hereinafter referred to as patent '690).

Patent '7404 disclose in the figures and respective portions of the specification an integrated circuit structure and an inherent method of packing a semiconductor device as claimed.

Referring to claims 1, 64, and 70, patent '7404 discloses an integrated circuit structure comprising:

a chip carrier 14 (socket);

at least one integrated circuit chip 16 containing structures which may be affected by external magnetic fields, said integrated circuit chip having a front surface and a back surface, said front surface being supported by said chip carrier and wherein said structures which may be affected by external magnetic fields may include a magnetic random access memory device;

a first magnetic field shielding material 18 (heat sink) in contact with said back surface of said chip; and

a second magnetic field shielding material 12 in contact with said chip carrier, such that said magnetic random access memory device is located between said first and second magnetic field shielding materials .

Note that although patent' 7404 does not disclose that the integrated circuit (IC) includes a magnetic random access memory device, magnetic random access memory device is available at the time the invention was made and the language that patent '7404 uses (electronic packages, microprocessor) includes magnetic random access memory device, and there is nothing in the reference of patent '7404 that teaches away the use of a magnetic random access memory device in the IC.

Note also that although the objective of patent '7404 is to minimizing EMI (outward) leakage, it is known that the shield works both ways: it prevents EMI from leaking out and it also prevents EMI from leaking in. It has also been held that a recitation (e.g., which shields said die from external magnetic fields) with respect to the manner in which a claimed apparatus is intended to be employed does not differentiate the claimed apparatus from a prior art apparatus satisfying the claimed structural limitations. *Ex Parte Masham*, 2 USPQ F.2d 1647 (1987).

Referring to claim 2, said first shielding material 18 is in the form of a first layer of said magnetic field shielding material on said back surface.

Referring to claim 11, said chip carrier 14 is a flip-chip carrier (since chip 16 is a flip-chip).

Referring to claims 19-23, 27, 64-65, and 71-76, patent '7404 discloses a chip/chip carrier 10 being mounted on a printed circuit board (PCB) 72 (Figures 3 and 4 and column 5, last full paragraph). However, patent '7404 fails to teach that PCB 72 is in contact with an additional layer of magnetic field shielding material (second layer or third layer as recited by the claims of the present invention) and a fourth layer of magnetic field shielding material and that this additional layer of magnetic field shielding material and the fourth layer of magnetic field shielding material is in contact with an upper surface and/or a bottom surface and/or embedded within the PCB. Nevertheless, the use of layers of magnetic field shielding material in and around PCBs for the purpose of shielding EMI (electromagnetic interference) is known in the art. For example:

- Patent '489 discloses a PCB capable of preventing EMI utilizing patterned metal layers in and around the PCB (Abstract).

- Patent '989 discloses in column 2, starting on line 32 that:

"In some instances, entire circuit boards are covered with a grounded lid. Polymer thick film conductor materials, such as a screen-printable copper filled epoxy paste, are sometimes used to form a shield. In other known EMI shielding methods, individual ferrite components are often placed on device pins or in series with a circuit to attenuate unwanted noise which may be causing system errors, or acting as sources of radiated emissions. In another application of ferrite beads or elements, a ferrite component is used with a capacitor in order to form a low frequency inductance-capacitance (LC) band pass filter, effectively shorting unwanted signal frequency components to ground."; and

- Patent '226 discloses that in a PCB, a ground path positioned between respective input and output connections for providing an electromagnetic shield therebetween. (column 2, lines 50-65).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to form PCB 72 as disclosed by patent '7404 such that it is in contact with an additional layer of magnetic field shielding material (second layer or third layer as recited by the claims of the present invention) and a fourth layer of magnetic field shielding material and that this additional layer of magnetic field shielding material and the fourth layer of magnetic field shielding material is in contact with an upper surface and/or a bottom surface and/or embedded within the PCB 72. One would have been motivated to make such a modification in view of the suggestions of patent '489, patent '989 and patent '226 that patterned circuit layers of PCB is capable of preventing EMI, that individual ferrite components are often placed on device pins or in series with a circuit of a PCB to attenuate unwanted noise which may be causing system errors, and that ground paths formed between respective input and output connections is for providing an electromagnetic shield therebetween. Needless to say, at the time the invention was made, PCB having multiple metal layers and multiple-layered ground paths in different layers, including top, bottom, and embedded, is known in the art.

Referring to claims 3-8, 13-18, 24-26, 28-31, 66-69, 83-86, and 79-82, materials for the first shielding material is not disclosed by patent '7404, so are the materials for the second through fourth magnetic field shielding material layers of the proposed device described above. Nevertheless, materials for EMI (electromagnetic interference) shielding are known in the art.

See, for example, the above quoted passage of patent '989 ("individual ferrite components are often placed on device pins or in series with a circuit to attenuate unwanted noise which may be causing system errors"); the above cited practice of utilizing conductive circuit (metalization) layers between input and output connections for providing an electromagnetic shield, the teachings by patent '690 of using non-conductive ferrite materials, such as Mn--Zn-Ferrite, Ni--Zn-Ferrite, MnFeO, CuFeO, FeO, or NiFeO, for shielding non-volatile magneto-resistive memory devices from stray magnetic fields (Abstract) and that the ferrite materials could be articles (column 5, lines 55-60); the teachings of patent '1404 about the use of conductive particles in a thermally and electrically conductive plastic resin for the purpose of protecting integrated circuits from radio and electromagnetic interference (Abstract); and the teachings of patent '489 about the use of copper powder (Abstract).

3. Claims 1-8, 11, 13-31, 64-76, 83-86, and 79-82 are rejected under 35 U.S.C. 102(b) as anticipated by or, in the alternative, under 35 U.S.C. 103(a) as obvious over Mertol U.S. Patent 5,866,943 (patent '943), using common knowledge in the art or in view of patent '489, patent '1404, patent '989, patent '226, or patent '690.

Patent '943 disclose in the figures and respective portions of the specification an integrated circuit structure and an inherent method of packing a semiconductor device as claimed.

Referring to claims 1, 64, and 70, patent '943 discloses an integrated circuit structure comprising:

a chip carrier 22/36;

at least one integrated circuit chip 10 containing structures which may be affected by external magnetic fields, said integrated circuit chip having a front surface and a back surface, said front surface being supported by said chip carrier and wherein said structures which may be affected by external magnetic fields may include a magnetic random access memory device;

a first magnetic field shielding material 26 (heat spreader) in contact with said back surface of said chip; and

a second magnetic field shielding material 30 in contact with said chip carrier, such that said magnetic random access memory device is located between said first and second magnetic field shielding materials .

Note that although patent' 943 does not disclose that the integrated circuit (IC) includes a magnetic random access memory device, magnetic random access memory device is available at the time the invention was made and the language that patent '943 uses (integrated circuit, i.e., chip) includes magnetic random access memory device, and there is nothing in the reference of patent '943 that teaches away the use of a magnetic random access memory device in the IC.

Note also that although patent '943 only discloses that heat spreader 26, being electrically coupled to ground paths 16 and ground pads 14, forms an EMI shield about the IC (Abstract and column 7, last two paragraphs), exemplary horizontal trace conductors 30, being metallic conductive, inherently possess some degree of EMI shielding as is known or as disclosed by patent 489 and cited above.

Referring to claim 2, said first shielding material 26 is in the form of a first layer of said magnetic field shielding material on said back surface.

Referring to claim 11, said chip carrier 22/36 is a flip-chip carrier (since chip 10 is a flip-chip).

Referring to claims 19-23, 27, 64-65, and 71-76, the grid array device package comprising chip 10 and chip carrier 22/36 requires to be connected to a PCB to function. However, patent '943 fails to explicitly disclose a PCB and fails to disclose that the PCB is in contact with an additional layer of magnetic field shielding material (second layer or third layer as recited by the claims of the present invention) and a fourth layer of magnetic field shielding material and that this additional layer of magnetic field shielding material and the fourth layer of magnetic field shielding material is in contact with an upper surface and/or a bottom surface and/or embedded within the PCB. Nevertheless, the use of layers of magnetic field shielding material in and around PCBs for the purpose of shielding EMI (electromagnetic interference) is known in the art. For example:

- Patent '489 discloses a PCB capable of preventing EMI utilizing patterned metal layers in and around the PCB (Abstract).

- Patent '989 discloses in column 2, starting on line 32 that:

"In some instances, entire circuit boards are covered with a grounded lid. Polymer thick film conductor materials, such as a screen-printable copper filled epoxy paste, are sometimes used to form a shield. In other known EMI shielding methods, individual ferrite components are often placed on device pins or in series with a circuit to attenuate unwanted noise which may be causing system errors, or acting as sources of radiated emissions. In another application of ferrite beads or elements, a ferrite component is used

with a capacitor in order to form a low frequency inductance-capacitance (LC) band pass filter, effectively shorting unwanted signal frequency components to ground."; and

- Patent '226 discloses that in a PCB, a ground path positioned between respective input and output connections for providing an electromagnetic shield therebetween. (column 2, lines 50-65).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to form a PCB, which is required by the device of patent '943 to function, such that it is in contact with an additional layer of magnetic field shielding material (second layer or third layer as recited by the claims of the present invention) and a fourth layer of magnetic field shielding material and that this additional layer of magnetic field shielding material and the fourth layer of magnetic field shielding material is in contact with an upper surface and/or a bottom surface and/or embedded within the PCB. One would have been motivated to make such a modification in view of the suggestions of patent '489, patent '989 and patent '226 that patterned circuit layers of PCB is capable of preventing EMI, that individual ferrite components are often placed on device pins or in series with a circuit of a PCB to attenuate unwanted noise which may be causing system errors, and that ground paths formed between respective input and output connections is for providing an electromagnetic shield therebetween. Needless to say, at the time the invention was made, PCB having multiple metal layers and multiple-layered ground paths in different layers, including top, bottom, and embedded, is known in the art.

Referring to claims 3-8, 13-18, 24-26, 28-31, 66-69, 83-86, and 79-82, the material for the first shielding material disclosed by patent '943 is a metal ("[H]eat spreader 26 is a plate

formed from an electrically and thermally conductive material (e.g., a metal such as aluminum), and of course the materials for the second through fourth magnetic field shielding material layers of the proposed device described above are not mentioned. Nevertheless, materials for EMI (electromagnetic interference) shielding are known in the art. See, for example, the above quoted passage of patent '989 ("individual ferrite components are often placed on device pins or in series with a circuit to attenuate unwanted noise which may be causing system errors"), the above cited practice of utilizing conductive circuit (metalization) layers between input and output connections for providing an electromagnetic shield; the teachings by patent '690 of using non-conductive ferrite materials, such as Mn--Zn-Ferrite, Ni--Zn-Ferrite, MnFeO, CuFeO, FeO, or NiFeO, for shielding non-volatile magneto-resistive memory devices from stray magnetic fields (Abstract) and that the ferrite materials could be articles (column 5, lines 55-60); the teachings of patent '1404 about the use of conductive particles in a thermally and electrically conductive plastic resin for the purpose of protecting integrated circuits from radio and electromagnetic interference (Abstract); and the teachings of patent '489 about the use of copper powder (Abstract).

4. Claims 1-8, 11, 13-31, 64-76, 83-86, and 79-82 are rejected under 35 U.S.C. 102(b) as anticipated by or, in the alternative, under 35 U.S.C. 103(a) as obvious over patent '1404), using common knowledge in the art or in view of patent '489, patent '690, patent '989, or patent '226.

Patent '1404 disclose in the figures and respective portions of the specification an integrated circuit structure and an inherent method of packing a semiconductor device as claimed.

Referring to claims 1, 64, and 70, patent '1404 discloses an integrated circuit structure comprising:

a chip carrier 10;

at least one integrated circuit chip 16 containing structures which may be affected by external magnetic fields, said integrated circuit chip having a front surface and a back surface, said front surface being supported by said chip carrier and wherein said structures which may be affected by external magnetic fields may include a magnetic random access memory device;

a first magnetic field shielding material 20 (thermally and electrically conductive plastic material) in contact with said back surface of said chip; and

a second magnetic field shielding material (17, among other hidden or not-shown metallized electrically conductive layer (metallization pattern)) in contact with said chip carrier, such that said magnetic random access memory device is located between said first and second magnetic field shielding materials . ("[T]he conductive plastic material is electrically connected to the circuit ground to shield the semiconductor device from radio frequency energy", SUMMARY OF THE INVENTION).

Note that although patent' 1404 does not disclose that the integrated circuit (IC) includes a magnetic random access memory device, magnetic random access memory device is available at the time the invention was made and the language that patent '1404 uses (IC, flip-chip) includes magnetic random access memory device, and there is nothing in the reference of patent '1404 that teaches away the use of a magnetic random access memory device in the IC.

Referring to claim 2, said first shielding material 20 is in the form of a first layer of said magnetic field shielding material on said back surface.

Referring to claim 11, said chip carrier 10 is a flip-chip carrier.

Referring to claims 19-23, 27, 64-65, and 71-76, the IC package 5 comprising flip-chip 16 and flip-chip carrier 10 requires to be connected to a PCB to function. However, patent '1404 fails to explicitly disclose a PCB and fails to disclose that the PCB is in contact with an additional layer of magnetic field shielding material (second layer or third layer as recited by the claims of the present invention) and a fourth layer of magnetic field shielding material and that this additional layer of magnetic field shielding material and the fourth layer of magnetic field shielding material is in contact with an upper surface and/or a bottom surface and/or embedded within the PCB. Nevertheless, the use of layers of magnetic field shielding material in and around PCBs for the purpose of shielding EMI (electromagnetic interference) is known in the art. For example:

- Patent '489 discloses a PCB capable of preventing EMI utilizing patterned metal layers in and around the PCB (Abstract).

- Patent '989 discloses in column 2, starting on line 32 that:

"In some instances, entire circuit boards are covered with a grounded lid. Polymer thick film conductor materials, such as a screen-printable copper filled epoxy paste, are sometimes used to form a shield. In other known EMI shielding methods, individual ferrite components are often placed on device pins or in series with a circuit to attenuate unwanted noise which may be causing system errors, or acting as sources of radiated emissions. In another application of ferrite beads or elements, a ferrite component is used

with a capacitor in order to form a low frequency inductance-capacitance (LC) band pass filter, effectively shorting unwanted signal frequency components to ground."; and

- Patent '226 discloses that in a PCB, a ground path positioned between respective input and output connections for providing an electromagnetic shield therebetween. (column 2, lines 50-65).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to form a PCB, which is required by the device of patent '1404 to function, such that it is in contact with an additional layer of magnetic field shielding material (second layer or third layer as recited by the claims of the present invention) and a fourth layer of magnetic field shielding material and that this additional layer of magnetic field shielding material and the fourth layer of magnetic field shielding material is in contact with an upper surface and/or a bottom surface and/or embedded within the PCB. One would have been motivated to make such a modification in view of the suggestions of patent '489, patent '989 and patent '226 that patterned circuit layers of PCB is capable of preventing EMI, that individual ferrite components are often placed on device pins or in series with a circuit of a PCB to attenuate unwanted noise which may be causing system errors, and that ground paths formed between respective input and output connections is for providing an electromagnetic shield therebetween. Needless to say, at the time the invention was made, PCB having multiple metal layers and multiple-layered ground paths in different layers, including top, bottom, and embedded, is known in the art.

Referring to claims 3-8, 13-18, 24-26, 28-31, 66-69, 83-86, and 79-82, the material for the first shielding material disclosed by patent '1404 is a metallic element or alloy (column 4,

first paragraph), and of course the materials for the second through fourth magnetic field shielding material layers of the proposed device described above are not mentioned. Nevertheless, materials for EMI (electromagnetic interference) shielding are known in the art. See, for example, the above quoted passage of patent '989 ("individual ferrite components are often placed on device pins or in series with a circuit to attenuate unwanted noise which may be causing system errors"); the above cited practice of utilizing conductive circuit (metalization) layers between input and output connections for providing an electromagnetic shield; the teachings by patent '690 of using non-conductive ferrite materials, such as Mn--Zn-Ferrite, Ni--Zn-Ferrite, MnFeO, CuFeO, FeO, or NiFeO, for shielding non-volatile magneto-resistive memory devices from stray magnetic fields (Abstract) and that the ferrite materials could be articles (column 5, lines 55-60); and the teachings of patent '489 about the use of copper powder (Abstract).

Conclusion

5. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

a. Youker et al. U.S. Patent 6,288,344 disclose an integrated EMI shield wherein the effective shielding is both vertical and horizontal to the chip.

6. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Tu-Tu Ho whose telephone number is (703) 305-0086. The examiner can normally be reached on 6:30 am - 5:00 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, DAVID NELMS can be reached on (703) 308-4910. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 308-7722 for regular communications and (703) 308-7722 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-1782.

Tu-Tu Ho
May 03, 2003

HOAI HO
PRIMARY EXAMINER